

# RC6601 Voltage Programmable Video Filter

# Features

- 250 kHz to 10 MHz minimum programmable range
- Precision factory-trimmed cutoff frequency of 5.5MHz
- Approximates CCIR601 digital video standard
- · Phase corrected for minimum group delay variation
- · External voltage or current control of cutoff frequency
- 0.25 % differential gain,  $R_L = 150\Omega$
- $0.20^{\circ}$  differential phase,  $R_L = 150\Omega$
- Minimum external components required
- Single ended input/output
- ±5V power supply
- 16-pin SOIC package

# Applications

- Video filtering
- Communication filters
- ADC anti-aliasing filter
- HDTV
- Set top boxes
- Satellite modems

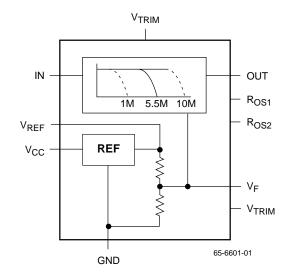
# Description

The RC6601 is a fully integrated continuous time filter, designed for various video filtering applications. The RC6601 approximates the requirements of the CCIR601 standard for digitizing NTSC and PAL video signals. It provides factory-set pass band ripple of  $\pm 0.25$  dB typical up to 5.5 MHz with a -40 dB stop band, beginning at 8 MHz.

The structure of the filter assures wide dynamic range operation with low noise and low distortion. The cutoff frequency is factory set at 5.5 MHz ( $\pm$ 5% typical). It can be varied over a range of 250 kHz–10 MHz by a user supplied voltage VF. The voltage VF can be readily derived from the on-chip precision reference voltage VREF as shown in the typical application circuit.

The RC6601 is packaged in a 300 mil wide body, 16-pin SOIC package. The package dimensions are included in this data sheet.

# **Block Diagram**

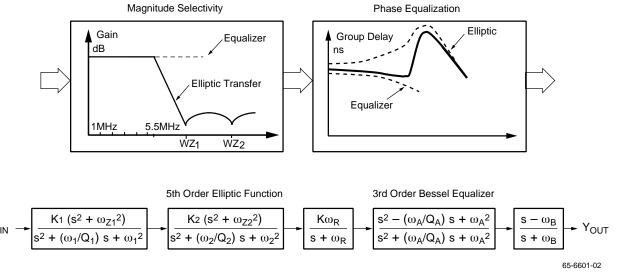


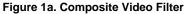
# **Functional Description**

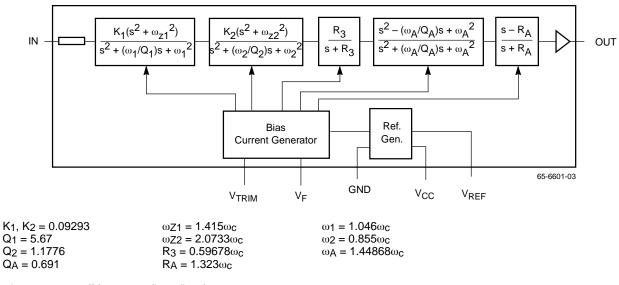
Digitizing video signals requires high-order anti-aliasing filters that can handle large signal swings with low distortion. CCIR601 standards recommend equi-ripple gain and group delay characteristics for filtering NTSC and PAL signals. RC6601 is a single-chip solution that matches the requirements with less than  $\pm 0.25$ dB gain ripple,  $\pm 20$ ns group delay variation in the passband, and more than 40dB attenuation in the stop band. The block diagram in Figure 1a shows the direct synthesis of the filter transfer function as a fifth order elliptic with third order phase equalization. The cut-off frequency, nominally set at 5.5MHz, is continuously programmable over a decade. Using current mode techniques, the IC can drive 2Vpp signals into 75 $\Omega$  load drawing only 35mA quiescent current.

The architecture of the complete filter as illustrated by Figure 1a is a 5th-order elliptic transfer function in tandem with a 3rd-order all-pass phase equalizer. The Cauer-elliptic response function has an equi-ripple passband with a sharp roll-off into stop-band in the magnitude transfer function but causes excessive group delay peaking. The equalizer maintains this magnitude response while compensating for the group delay peaking. These two filters are represented in Figure 1a by a series of 2nd-order expressions that can be realized as biquads using transimpedance-based integrators. Elliptic poles and zeros give a flat magnitude response in passband and a 40dB roll-off from 5.5MHz to 8MHz. The equalizer transfer function corrects group delay to  $\pm 15$ ns to 90% of the cut-off frequency. These pole-zero values determine biquad coefficients as shown in Figure 1b. A supplyindependent band-gap cell generates and distributes bias currents for all the transimpedance integrators as in Figure 1b. The cut-off frequency is programmed by globally scaling the currents, using a single external setting.

The entire filter, including the programmable bias generators, is integrated on a single chip using complementary bipolar technology. The npn and pnp transistors have a cutoff frequency of 4GHz and of 1.5GHz respectively. Gateoxide-based capacitors and thin film resistors with 0.5% match set filter time constants. At 5.5MHz cut-off, the filter averages 2.5mA/pole. Nearly 15mA of the supply current is used for the output driver. The cut-off frequency is actually programmable beyond the 1–10 MHz, with an external voltage control. Measured differential gain of 0.25% and a differential phase of 0.2° make it well suited for video applications.







where  $\omega_c$  = cut off frequency (in radians) e.g. for default filter:  $\omega_c = 2\pi \cdot (5.5)10^6 = 34.5575 \times 10^6$ Scaling bias currents directly scales the frequency  $\omega_c$ 

#### Figure 1b. Internal Programming Architecture

### **Pin Assignments**

$V_{EE1}$	1	16	V <sub>CC</sub>
IN	2	15	OUT
V <sub>COM</sub>	3	14	$V_{EE2}$
NC	4	13	V <sub>TRIM</sub>
NC	5	12	R <sub>OS2</sub>
NC	6	11	R <sub>OS1</sub>
GND	7	10	NC
$V_{REF}$	8	9	VF
		65-6601-04	

### **Pin Descriptions**

Pin Name	Pin Number	Description
GND	7	Supply Ground
IN	2	Signal Input
NC	4–6, 10	No Connect
OUT	15	Signal Output
ROS1	11	Offset Adjust 1
ROS2	12	Offset Adjust 2
Vcc	16	Positive Supply Voltage
VCOM	3	Common Mode Input Voltage (See Note)
VEE1	1	Negative Supply Voltage (Input Section)
VEE2	14	Negative Supply Voltage (Output Section)
VF	9	Filter Control Voltage for Cut-off Frequency
Vref	8	Precision Reference Voltage
Vtrim	13	Pass Band Peaking Voltage

Note: V<sub>COM</sub> pin is typically connected to ground for ±5V supply.

# **Absolute Maximum Ratings**

(beyond which the device may be damaged)<sup>1</sup>

Parameter	Min.	Тур.	Max.	Units
Positive Power Supply (VCC)			6	V
Negative Power Supply (VEE1, VEE2)			-6	V
Input Voltage	(VEE1, VE	E2) -0.3 V to V	CC to +0.3V	V
Input Current (Power On or Off)			±10	mA
Operating Temperature	0		70	°C
Storage Temperature	-40		125	°C
Junction Temperature		150		°C
Lead Soldering (10 seconds)			300	°C
Short Circuit Tolerance	No more than one output may be shorted to grour			

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

# **Operating Conditions**

Parame	ter	Min.	Тур.	Max.	Units
Vcc	Power Supply Voltage	4.75	5.0	5.25	V
VEE	Negative Supply Voltage	-5.25	-5.0	-4.75	V
Is	Quiescent Supply Current		40	50	mA
θJA	SO16 Thermal Resistance		105		°C/W

# **DC Electrical Characteristics**

 $V_{CC} = 5V$ ,  $V_{EE1,2} = -5V$ ,  $C_L = 15pF$ ,  $R_L = 150\Omega$ ,  $T_A = 25^{\circ}C$ , unless otherwise specified.

Paramet	er	Conditions	Min.	Тур.	Max.	Units
Av	DC gain accuracy	VIN = 2 Vpp	0.90	1	1.10	V/V
Rin	Input resistance	DC		4		kΩ
lo	Output current			±10		mA
Voff	Output offset voltage	Without offset adjust	-500		+500	mV
		With offset adjust	-10		+10	mV
Vref	Reference voltage		2.30	2.48	2.60	V
IREF	Reference output current	Max reference out current		5		mA
VF	Frequency set voltage (FC = 5.5 MHz ±10%)	IF = 0, Measure VF		1.24		V
RF	Frequency set input resistance			5.0		kΩ

VCC = 5V, VEE1,2 = -5V, CL = 15pF, RL =  $150\Omega$ , fPB = 5.5 MHz, TA =  $25^{\circ}$ C, unless otherwise specified.

Parameter		Conditions	Min.	Тур.	Max.	Units
Filter Characteristics						
fрв	Passband frequency	VF ≈ 0V	10	15		MHz
		VF = VREF ≈ 2.5V	.25		1	MHz
fCA	Filter cutoff accuracy <sup>5,6</sup>	fPB = 5.5MHz	-5		+5	%
fCT	Filter cutoff drift <sup>5</sup>	fPB = 5.5MHz	-5		+5	%
∆tGD	Group delay flatness	fin = 100 kHz to 4,9 MHz		±20		ns
Vin	Input signal range	THD < 1 % <sup>(7)</sup>	1	2		Vpp
CIN	Input capacitance			10		pF
ΔG	Diff. gain, NTSC & PAL	VIN = 286 mVpp, 4.43 MHz		.25		%
ΔP	Diff. phase, NTSC & PAL	VIN = 286 mVpp, 4.43 MHz		.20		0
en	RMS output noise voltage	R <sub>S</sub> = 75 Ω, 10 MHz BW <sup>(7)</sup>		1.3	2.0	mV
SR	Positive slew rate <sup>3</sup>	V <sub>IN</sub> = 2 Vpp		60		V/µs
	Negative slew rate <sup>3</sup>	VIN = 2 Vpp		60		V/µs
Ro	Output resistance			3		Ω
ATT	Attenuation <sup>1</sup>	fin ≤ 5.0 MHz, VIN = 1 Vpp		±0.10	±0.25	dB
	Attenuation <sup>2</sup>	f <sub>in</sub> ≤ 5.0 MHz, V <sub>IN</sub> = 1 Vpp		±0.5	± 1	dB
	Attenuation <sup>2</sup>	fin = 6.75 MHz, VIN = 1 Vpp		-12	-8	dB
	Attenuation <sup>2</sup>	f <sub>in</sub> = 8 MHz, V <sub>IN</sub> = 1 Vpp		-40		dB
	Attenuation <sup>2</sup>	8 MHz < fin < 50 MHz, VIN = 1 Vpp		-40	-35	dB
	Attenuation <sup>1,4</sup>	f <sub>IN</sub> ≤ 2.5 MHz, V <sub>IN</sub> = 1 Vpp		±0.10	±0.25	dB
	Attenuation <sup>2,4</sup>	fIN ≤ 2.5 MHz, VIN = 1 Vpp		±0.5	± 1	dB
	Attenuation <sup>2,4</sup>	f <sub>IN</sub> = 3.375 MHz, V <sub>IN</sub> = 1 Vpp			-8	dB
	Attenuation <sup>2,4</sup>	fIN = 4 MHz, VIN = 1 Vpp		-40		dB
	Attenuation <sup>2,4</sup>	4 MHz < f <sub>IN</sub> < 50 MHz, V <sub>IN</sub> = 1 Vpp			-35	dB
SPW	Sensitivity of cutoff frequency vs. supply voltages	VS = ±5 V, VF = 1.25 V		1		%/V

- 1. VTRIM adjusted for optimum response.
- 2. No external adjustments.
- 3. Guaranteed no slew limit on 2V p-p input at 9 MHz.
- 4. Filter programmed for 2.75 MHz cutoff,  $V_F = 1.85V$ .
- 5. Filter cutoff defined to edge of ripple spec.
- 6. Initial setpoint accuracy of cutoff, excluding temperature and long term drift.
- 7. Guaranteed by design.

### **Performance Curves**

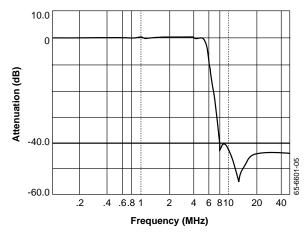


Figure 2. Amplitude Response—Default Setting

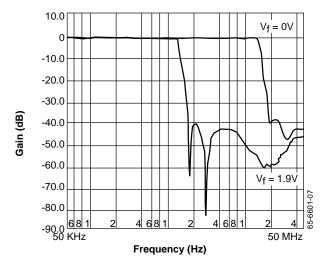


Figure 4. Amplitude Responses Over Programming Range

# **Application Discussion**

The RC6601 is fully integrated in the sense that no critical external components are required for the low pass filtering function. For luminance filtering at a cut-off frequency of 5.5MHz, the only off-chip components are the decoupling capacitors and termination resistors shown in Figure 6. The part also provides temperature and supply independent band-gap reference voltages (2.48V and 1.24V) that can be used for setting the ADC converters or DACs in the system.

The programmable feature of the RC6601 makes it versatile for use in applications with other standard cut-off frequencies. There are three ways of changing the cut-off frequency.

1. **External Voltage setting on VF:** A higher voltage on VF than 1.2V gives a lower frequency than 5.5MHz cutoff. The highest frequency (above 10MHz) is obtained by grounding the VF pin.

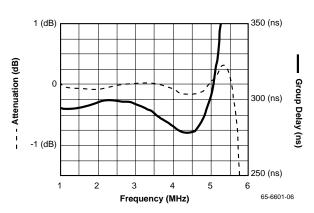


Figure 3. Attentuation and Group Delay

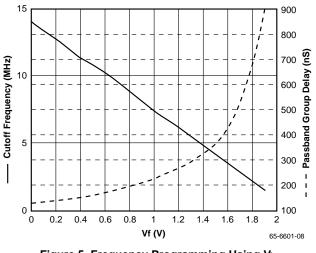


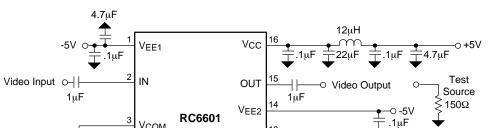
Figure 5. Frequency Programming Using V<sub>f</sub> and Passband Group Delay

- 2. Potentiometer at VREF (pin 8) and/or VF (pin 9): There is an internal resistor divider of roughly 10K each that sets the default voltage of 1.2V at half the value of VREF. Using a lower value external pot of 1K-2K, the internal setting can be overridden.
- Current Source/Sink at VF: The typical current output from a DAC can be tied to the VF pin to program the cut-off frequency from a controller.

In applications requiring dynamic programming of the filter cut-off, a combination of above techniques may be used. Use of the RC6601 in such applications eliminates the need for multiplexers and filter banks. The other adjustment possible on the RC6601 is the output d.c. level. The output d.c. level can be adjusted by connecting a potentiometer between pins ROS1 and ROS2 (pins 11 and 12) and taking the center tap to V<sub>CC</sub>. These adjustments are shown in Figure 7 below.

Test Source

-0



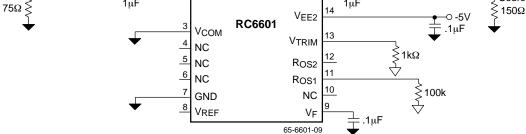


Figure 6. Fixed Configuration CCIR601 (Cutoff frequency is factory set to 5.5MHz)

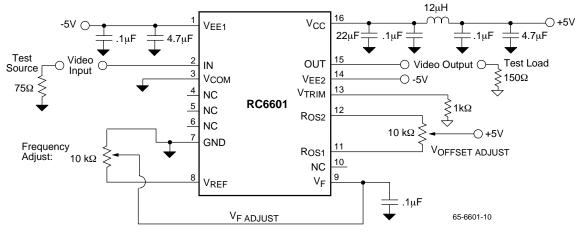
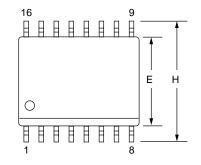


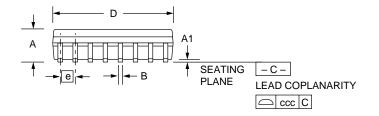
Figure 7. Cutoff Frequency and Offset Tunable Filter

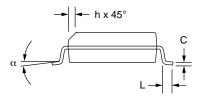
# Mechanical Dimensions – 16 Pin SOIC Package

Symbol	Inches		Millin	Notes	
Symbol	Min.	Max.	Min.	Max.	Notes
А	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
В	.013	.020	0.33	0.51	
С	.009	.013	0.23	0.32	5
D	.398	.413	10.10	10.50	2
Е	.291	.299	7.40	7.60	2
е	.050	.050 BSC		BSC	
Н	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
Ν	16		16		6
α	0°	8°	0°	8°	
CCC	_	.004	_	0.10	

- 1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- 3. "L" is the length of terminal for soldering to a substrate.
- 4. Terminal numbers are shown for reference only.
- 5. "C" dimension does not include solder finish thickness.
- 6. Symbol "N" is the maximum number of terminals.







### **Ordering Information**

Product Number	Temperature Range	Screening	Package	Package Marking
RC6601M	0° to 70°C	Commercial	16 Pin Wide SOIC	RC6601M

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